Process and characterization of 50 nm vertical double gate MOSFET (VDGM) with FILOX using TCAD tools

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In this paper, we propose a novel CMOS compatible fabrication process of vertical double gate MOSFETs (VDGM) with incorporation of FILOX. A systematic process simulation in realizing the VDGM structure in which the source and drain are self-aligned by 45°- tilt-ion-implantation TCAD process is reported. An NMOSFET device with 50 nm gate length, 3 nm gate oxide and 190 nm silicon thickness is observed by using vertical and horizontal doping profiles. With source and drain doping of 4×10^{20} cm^{-3} and body doping of 5×10^{18} cm^{-3}, a very low leakage current I_{OFF} = 2.32×10^{-15} A/μm and good drive current I_{ON} = 1.6×10^{-5} A/μm at V_{DS} = 0.025V was explicitly shown. I_{OFF} increases to 2.74×10^{-14} A/μm and I_{ON} to 1.8×10^{-4} A/μm for V_{DS} = 1.5 V. The threshold voltage, V_T were extracted to be 1.1 V and 0.8 V for V_{DS} = 0.025 V and 1.5 V respectively. The subthreshold characteristics also highlighted a reasonably well-controlled short channel effect (SCE) with subthreshold swing $SubV_T$ = 67.3 mV/dec at V_{DS} = 0.025 V that slightly increases to 81.9 mV/dec at V_{DS} = 1.5 V. In addition, the output characteristics illustrated a very good drain current at different gate voltage with increasing drain voltage. These results show that the vertical transistor is seen to offer considerable advantages down to the 100 nm node and beyond due to the dual or surround channels and the ability to produce a 50 nm channel length with relaxed lithography dependence.

I. INTRODUCTION

In recent years, there has been an increasing focus on vertical transistor due to its architecture that provides a simpler formation of double and even surrounding gate with sub-micron definition of channel length. The four main factors for developing vertical MOS transistors on the sidewalls of vertical pillars are [1]:

- The definition of gate length is controlled by non-lithographic methods that allow the realization of shorter channel length as compared to methods using photolithography.
- The realization of double or surround gate structure allow more channel width per unit of silicon area that leads to an increase of the drive current per unit area.
- This structure allows the decoupling of gate length from the packing density making a long channel transistor with lower off currents for RAM applications.
- The possibility of making very thin and fully depleted pillars with controllable substrate depletion regions that allow reduction of short channel effects (SCE).

In general, the vertical MOSFET can be categorized according to the gate length fabrication methods. One way is to use the expensive epitaxial growth such as Molecular Beam Epitaxy processes (MBE) [2-5]. The retarded etching [6] is another approach to defined the gate length. Another technique is to etch silicon pillars and then diffuse the implanted dopants without tilt angle to silicon pillar [7-10]. The major disadvantage of epitaxial and etching approaches is that they are not CMOS compatible. Ion implanted vertical MOSFET [11] use non-lithographic methods to define the gate length and hence are CMOS compatible. However, the minimum channel length that can be reached is limited by the height of silicon pillar dry etch and the thickness of nitride fillets. As a result, unacceptable high threshold voltage, large leakage current and unacceptable DIBL is observed for 125 nm device. This limits the scaling of such devices into nanometre regime. To address these problems, tilted ion implantation method was employed for making the self-aligned symmetrical source and drain regions over silicon pillar. In this way, a sharp vertical channel profile is produced over the pillar. Subsequently the current drivability and threshold voltage controllability will be improved in order to overcome the SCE. The characterization analysis of this method is performed using both the process and device simulation respectively [12].

II. DEVICE STRUCTURE AND PROCESS

The simulated VDGM structure is shown in Fig. 1. Prior to the device fabrication process, the mesh or grid of device size is defined so that the critical area such as

L_g, impurity regions and t_{ox} are given finer mesh as compared to others. The process starts with a boron-doped (100) silicon wafers as the starting material. The dry etch of the Si pillars to a height of about 200 nm using nitride masks is done. A 20 nm stress relief oxide was thermally grown using dry oxygen (30 s, 900°C) to relieve the stress between the ensuing nitride layer and the silicon. Using viscosity method the silicon nitride was deposited to a thickness of 130 nm. The active area was defined by patterning the nitride layer and stress relief oxide using an anisotropic dry etch. This results in the formation of 130 nm wide nitride spacers on the sidewalls of the pillars. Subsequently, a formation of FILOX took place by thermally grown 60 nm thick oxide layer (60 s, 1000°C). The area protected by the nitride spacers was not affected by the oxide growth; thus a thick oxide layer was formed on the whole active area and on the top of the pillar. The self-aligned source/drain regions were implanted using 45° tilt Arsenic (6×10^{15} cm^{-2}, 150 keV). After removing the nitride fillets, an isotropic wet etch for 1 minute followed by an anisotropic dry etch using previously defined photoresist is performed. The nitride mask is used to remove the stress relief oxide, leaving an approximately 40 nm thick FILOX oxide. A 3-nm gate oxide was thermally grown on the sidewall of the pillar at 800 °C for 10 s. Then a 200 nm in-situ doped (arsenic, 5×10^{19} cm^{-3}) polysilicon gate was deposited and patterned by dry etch. In this way n-type polysilicon spacers were created on the left and right of the pillar for double gate electrodes definition. A 100 nm thick oxide isolation layer was then deposited and an RTA at 1100°C for 0.17 s was performed for dopant activation. Finally contacts were etched and metal deposited and patterned.

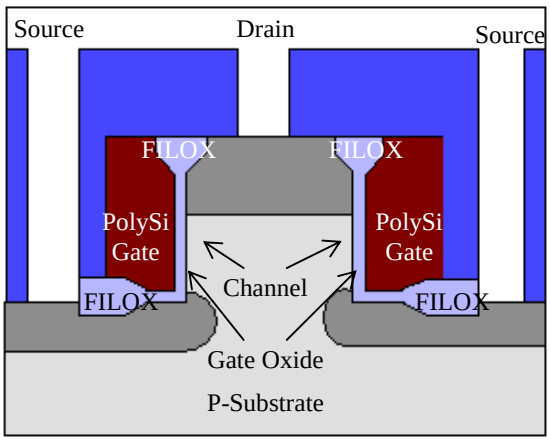

FIG. 1. Schematic structure of vertical double gate MOSFET (VDGM).

III. DEVICE PHYSICAL MODELS

Once the device structure is designed, the analysis on device characterization is needed. The device is represented as a meshed finite-element structure. For each node, the carrier concentration, current densities, electric field, generation and recombination rates, etc. are computed. The device simulator solves the Poisson equation, the carrier continuity equation, drift-diffusion and energy balance equation. The carrier statistics based on simplified Boltzmann equation is used. After solving these equations, the resulting electrical currents at the contacts are extracted and an output characteristics and I-V graphs are plotted. For the VDGM device characterization, the inversion layer mobility model from Lombardi [12] was employed for its dependency on the transverse field (i.e. field in the direction perpendicular $E_\perp$ to the Si/SiO_2 interface of the MOSFET) and through velocity saturation at high longitudinal field (i.e. field in the direction from source-to drain) combined with SRH (Shockley-Read-Hall Recombination) with fixed carrier lifetimes models. This recombination model was selected since it takes into account the phonon transition effect due to the presence of a trap (or defect) within the forbidden gap of the semiconductor. An interface fixed oxide charge of 3×10^{10} coulomb is assumed with n-type polysilicon gate contact for the device. The drift-diffusion transport model with simplified Boltzmann carrier statistics is employed for numerical computation of the design device.

IV. DOPING PROFILES

Fig. 2 shows the vertical doping profiles of VDGM device which is taken from the top drain region to body or channel region and the bottom source region. As indicated in Fig. 2 the effective channel length L_g was calculated to be 50 nm which is measured from the intercept points of arsenic and boron impurity to the left and right of the graph. Also visible in Fig. 2 are the flat doping profiles of body region of 5×10^{18} cm^{-3}, drain doping of 1×10^{19} cm^{-3} and source doping of 2×10^{-19} cm^{-3} that was self-aligned using tilt 45° ion implantation process. Therefore, by controlling the degree to which the implanted ion are bombard to silicon wafer the submicron gate length definition is possible which is independent of lithography process and is CMOS compatible.

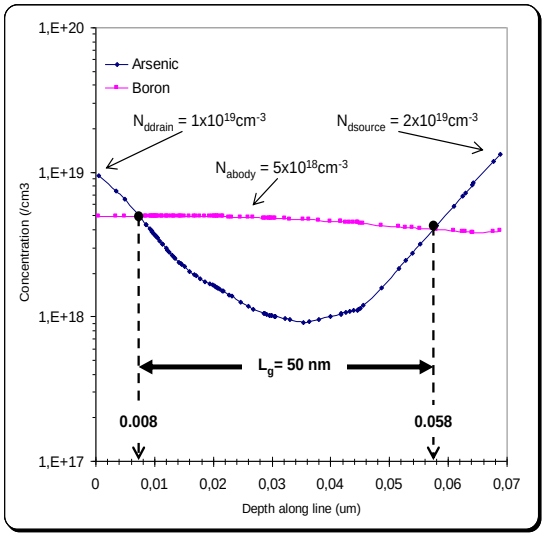

FIG. 2. Vertical doping profiles of design VDGM with L_g = 50 nm, drain doping, $N_{ddrain} = 1\times10^{19}$ cm^{-3}, source doping, $N_{dsource} = 2\times10^{19}$ cm^{-3} and body doping, $N_{abody} = 5\times10^{18}$ cm^{-3}.

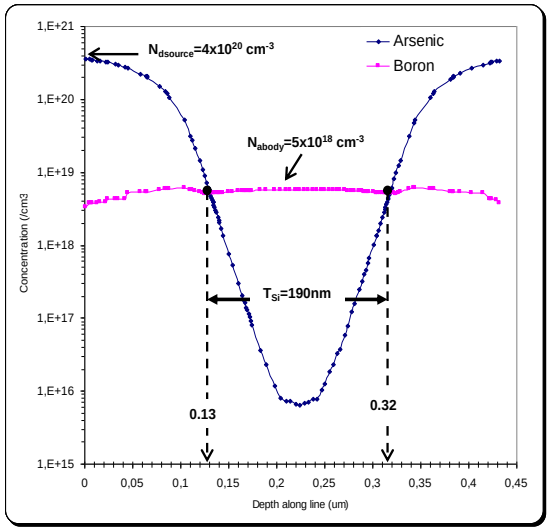

FIG. 3. Horizontal doping profiles of design VDGM with silicon thickness t_{si} = 190 nm , drain doping, $N_{ddrain} = 4\times10^{20}$ cm^{-3}, source doping, $N_{dsource} = 4\times10^{20}$ cm^{-3} and body doping, $N_{abody} = 5\times10^{18}$ cm^{-3}.

To further analyze the VDGM device, the horizontal doping profile was taken as shown in Fig. 3. The profile was taken from the left source region to the body area and finally to the right of source region. This profile is used to further validate the doping level of drain, source and body region since it was an important factor for adjusting the threshold voltage V_T of the device. Thus from Fig. 3, the source and drain doping was validated to be 4×10^{20} cm^{-3} and the body doping to be 5×10^{18} cm^{-3}. The high body doping is necessary to control the short channel effect (SCE) and setting the V_T properly [13]. However, the trade-off between controlling SCE and reducing leakage current I_{OFF} was essential [14]. Due to high channel doping the mobility of holes and electrons will be reduced and the junction leakage due to band-to-band tunneling and gate-induced drain leakage (GIDL) will increase. The silicon thickness t_{Si} = 190 nm is noted in Fig. 3. This parameter is important in distinguishing the operation of partly depleted (PD) and fully depleted (FD) MOSFET. In FD double or even surround gate vertical MOSFETs, the SCE are controlled by the gate voltage so that it is not necessary to increase the body doping while reducing the channel length. This allows bypassing the problem of increased leakage current due to body/drain tunnelling with higher body doping.

V. ELECTRICAL CHARACTERIZATION

The combination of Gummel and Newton numerical methods was employed for a better initial guess in solving quantities for obtaining a convergence of the device structure. Fig. 4 shows the transfer or current-voltage (I_{GS} – V_{GS}) characteristics of the device with channel length L_g = 50 nm, oxide thickness t_{ox} = 3.0 nm and body doping $N_{abody} = 5.0\times10^{18}$ cm^{-3}. By using a linear extrapolation of transconductance g_m (V_{GS}) to zero [15] a 1.1 V threshold voltage V_T was obtained at V_{DS} = 0.025 V and reduced to 0.8 V at V_{DS} = 1.5 V. The moderately high V_T was expected since the device has two channels with double gate thus a high gate voltage V_{GS} is needed for inverting the dual p-type body channel doping. In addition, these values are consistent with the fabrication device by Enrico Gili *et al.* [11] in which the V_T for double gate is 1.54 V for V_{DS} = 0.025 V and decreases to 1.44 at V_{DS} = 1.0 V for L_g = 125 nm. However an improved lower V_T is possibly due to self-aligned S/D and sharp vertical channel obtained by tilted ion implantation method. The dependence of V_T on drain voltage that decreased from 1.1 V at V_{DS} = 0.025 V to 0.8 V at V_{DS} = 1.5 V was due to Drain-Induced-Barrier Lowering (DIBL) effect. This effect mainly reduces the controllability of channel by the gate as channel length is scaled down due to larger electric field as drain voltage increased. The DIBL (defined as $V_{T(Vds=0.025V)} - V_{T(Vds=1.5V)}$) is calculated to be 203 mV/V and 103 mV/V for L_g = 50 nm and 125 nm respectively. It shows an aggravated SCE that increased by a factor of 2 compared with fabricated device.

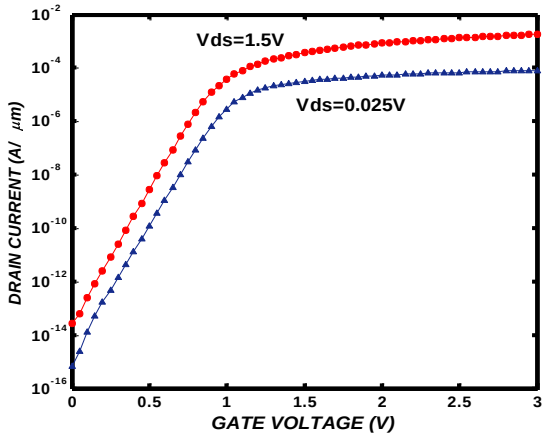

FIG. 4. Transfer characteristic of VDGM device with L_g = 50 nm, T_{OX} = 3 nm, $N_{abody} = 5\times10^{18}$ cm^{-3}; $V_S = V_B = 0$ V.

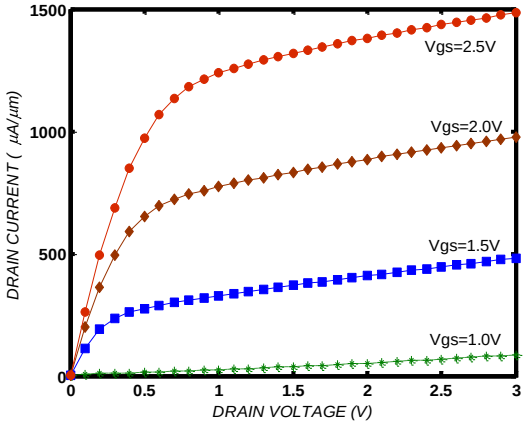

FIG. 5. Output characteristic of VDGM with L_g = 50 nm, T_{OX} = 3 nm, $N_A = 5\times10^{18}$ cm^{-3} for V_{GS} = 1, 1.5, 2 and 2.5 V.

In the off-state operation mode the transistors show a drain leakage current I_{OFF} which is independent of the gate voltage, but increases with increasing drain voltage as depicted in Fig. 4. A very low off-state leakage current $I_{OFF} = 2.32\times10^{-15}$ A/μm and good drive current $I_{ON} = 1.6\times10^{-5}$ A/μm at V_{DS} = 0.025 V was explicitly shown. It increases to $I_{OFF} = 2.74\times10^{-14}$ A/μm and $I_{ON} = 1.8\times10^{-4}$ A/μm for V_{DS} = 1.5 V. The off-state drain current I_{OFF} was measured at V_{GS} = 0 V and the on-state drain current is measured when $V_{GS} - V_T = 1$ V. To find the origin of this leakage, the currents from all electrodes of the devices have been measured simultaneously. This shows that the leakage current originates from the reverse biased drain-substrate diode. Due to a good OFF/ON ratio of the devices, the subthreshold characteristics are also highlighted. A reasonably well-controlled SCE with subthreshold swing $SubV_T$ = 67.3 mV/dec at V_{DS} = 0.025V with slight increase to 81.9 mV/dec at Vds = 1.5 V is observed. The output $I_{DS} - V_{DS}$ characteristics for V_{GS} = 1.0, 1.5, 2.0 and 2.5 are shown in Fig. 5. Due to the double gate configuration the drain current shows an acceptable value from the minimum of 200 μA/μm to a maximum of 1500 μA/μm at V_{DS} = 1 V and 2.5 V respectively.

VI. CONCLUSIONS

For the first time the fabrication process of 50 nm Vertical Double Gate MOSFET (VDGM) device has been successfully done using commercial ATHENA TCAD tools. This was achieved by the utilization of tilt 45° ion implantation in defining the region of self-aligned source and drain. Therefore, by controlling the degree to which the implanted ion are bombard to silicon wafer the submicron gate length definition is possible which is independent of lithography process and is CMOS compatible. By employing the inversion layer mobility model from Lombardi combined with SRH (Shockley-Read-Hall Recombination) with fixed carrier lifetimes' models, a detailed investigation on the VDGM performance was done. With the gate length of 50 nm, body doping of 5×10^{18} cm^{-3} and oxide thickness, t_{ox} = 3 nm, a good drive current I_{ON} of 16 μA/μm and a low off-state leakage current $I_{OFF} = 2.32\times10^{-15}$ A/μm was obtained. In addition, the subthreshold characteristics also highlighted a reasonably well-controlled SCE with subthreshold swing $SubV_T$ = 67.3 mV/decade and threshold voltage V_T = 1.1 V. Thus with the simulation results, we can conclude that this device shows a possibility of extending the silicon based device beyond nanometer regime for the future demand of smaller-size electronic products.

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