Creating the IBIS model for a digital IC device

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IBIS model has gained popularity over SPICE model among the system designers over the last two decades. This is because the latter suffers from some practical realities such as undocumented simplifications and model availability as well as proprietorship issue. Yet it is important to have an accurate device model for system and circuit analysis and design. This paper reports on the results of the IBIS model created for a 24 pins digital IC device following the guidelines of the IBIS Open Forum.

I. INTRODUCTION

Simulation to study the behavior of a design before prototyping has become an inevitable part of the system designing. Modeling in turn provides the system designers with the tool to do the simulation. Spice simulation has long been the primary method for system and circuit analysis and design. However, it suffers from some practical realities such as different simulators, undocumented simplifications, simulation speed, model availability, etc. Most importantly, to get the best models for the spice simulation very often clashes with the issue of proprietorship of the semiconductor vendors to the point that the semiconductor manufacturers are reluctant to provide the spice model of I/O structure to the public, thus rendering the spice-based models a weak link when design complexity increases. This issue has been resolved with the adoption of IBIS as a new standard for modeling [1,2].

The Input/output Buffer Information Specification (IBIS) was developed at Intel Corporation in the early 1990s and has now become more and more popular among the system designers. Several versions of IBIS have been published since then. Version 1.0 in which described CMOS and TTL I/O buffers was issued in June 1993 and soon after that a clarification update, Version 1.1, was issued in August the same year. Version 2.0 was ratified on June 1994, and similarly an updated version, Version 2.1, in February 1995. IBIS became an American National Standard ANSI/EIA-656 in December the same year. IBIS Version 3.2 was ratified on September 1999 and renewed in August 2005 as ANSI/EIA-656-A. Version 4.0 was ratified on July 2002, and Version 4.2 was ratified as ANSI/EIA-656-B on September 2006 [3,4]. Note that all versions of IBIS are compatible with one another with each version adds and supports new capabilities, technologies and device types. Together with this development was the formation of the IBIS Open Forum in 1993. The committee supplies information and development tools and promotes IBIS model development and distribution [3].

IBIS model describes the electrical characteristics of the digital inputs and outputs of a device. In the model, the behavior of the device is represented by a set of tabular data of current and voltage values in the input and output pins, and the voltage and time relationship at the output pins under switching conditions, from low level to high level and from high level to low level. The IBIS model is normally created in the following three steps. The first step is to collect the current and voltage data of the device. This can be obtained through lab measurements. Note that in this measurement, if the device is a nominal device, then a typical IBIS model would be obtained. After that the data is put into the IBIS file which is formatted in ASCII text. An IBIS file is not an executable file but a file that collects all the data describing the electrical characteristics of the device and can be used in a simulator. The third step is to validate the model. This is first done using the Golden Parser, also known as ibischk3 [2], which is used to check that the syntax and structure of the IBIS file follow the standard; and then the current-voltage (I/V) and Voltage-time (V/T) curves generated should be visually inspected and make sure that the results are as expected.

This paper reports the result of the IBIS model created for a 24 pins digital IC based on the processes described in the last paragraph.

II. IBIS MODEL OVERVIEW

The output model of IBIS is characterized by dc electrical data, switching data and device parameters, which are represented schematically by a PMOS Pull-up transistor, a NMOS Pull-down transistor, two diodes for ESD protection, the die capacitance (C_comp) and the package parasitic [1,2]. Fig. 1 shows the schematic diagram of the IBIS output buffer model. The pull-up data describes the I/V behavior when the output is in a logic high state (corresponding to PMOS transistor ON), and pull-down data when output is in logic low state (NMOS transistor ON). The power and clamp data represent the electrical behavior of the output when the output is above Vcc and when the output is below ground respectively. C_comp in the schematic represents

the die capacitance and the package parasitic is represented by R_pin, L_pin and C_pin, the electrical characteristics of resistance, inductance and capacitance for each pin-to-buffer connection. Not usually shown in the schematic is the switching characteristic of the buffer. The ramp rate, dV/dt describes the transition time when the output switches from one state to another. It is measured from the 20% to the 80% of Vcc points with a default resistive load of 50 ? [4].

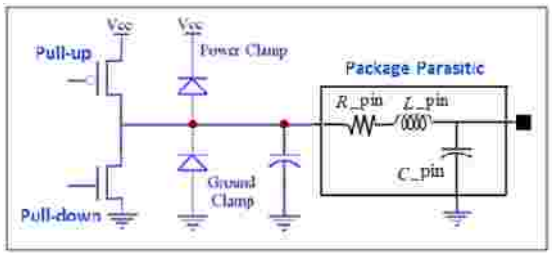

FIG. 1. Schematic of IBIS output buffer model.

The input buffer model of IBIS is represented schematically by the package parasitic, the die capacitance, the power and ground clamp as shown in Fig. 2.

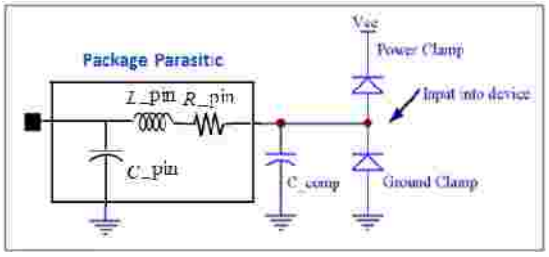

FIG. 2. Schematic of IBIS input buffer model.

IBIS also specifies the ranges of the sweep voltages for the pull-up data, pull-down data, power clamp data and the ground clamp data as shown in Table I [3].

TABLE I. Ranges of sweep voltage for each I/V characteristics.

I/V characteristics	Ranges of sweep voltage
Pull-up	-Vcc to 2Vcc
Pull-down	-Vcc to 2Vcc
Power clamp	-Vcc to Vcc
Ground clamp	+Vcc to 2Vcc

III. CREATING THE IBIS MODEL

The Tektronix 370A Programmable Curve Tracer was used for the current and voltage data collection using the grounded-emitter configuration. The curve tracer was connected directly to a computer to transfer the captured I/V curves from curve tracer to the computer using the CAP (Curve Tracer Acquisition Program) software which allows for enhanced visualization of the uploaded I/V curve. The actual data is presented in a text file consisting of two columns, one for current and one for voltage.

The physical dimension of the Device under Test (DUT) is very small and the pins are very close together. Thus, an evaluation board (EVB) specially engineered for this device family was used to provide contact between the probe of the curve tracer and the individual pins on the chip. The chip was inserted into a socket on the DUT board which was mounted on the socket in the middle of the EVB. The DUT pins are connected to the pad on the DUT board and each pad is connected to a (larger) pin on the EVB. The EVB was then connected to the computer using a interface board. This interface board is necessary because a code will be downloaded into the DUT memory to set the particular output pins into a high state or a low state when measurements were performed. Last but not least a programmable power supply with output capability to sink and source current was used to power the EVB and the DUT. The power supply supplies two voltages to the EVB, 1.8V for the core voltage and 3.3V for the independent input/output power.

Table II summarizes the ranges of voltage sweep to obtain the various I/V curves as defined in IBIS specification. For this device, Vcc is 3.3V [5]

TABLE II. Ranges of sweep voltage for each I/V characteristics.

I/V characteristics	Ranges of sweep voltage
Pull-up	-3.3V to 6.6V
Pull-down	-3.3V to 6.6V
Power clamp	3.3V to 4.2V*
Ground clamp	-3.3V to 3.3V

*Note that due to the limitation of the equipment here, the upper limit voltage could only reach 4.2V (instead of the 6.6V) in these measurements.

IIIa. The Power and Ground Clamp I/V Curves

In this measurement, both the power clamp and ground clamp curves were obtained at the same time by a single voltage swept from -Vcc to +2Vcc. However, due to the limitation of the equipment here, the upper limit voltage could only reach 4.2V (instead of the 6.6V). This clamp curve was then separated into the Power Clamp data (Fig. 3) and Ground Clamp data (Fig. 4) based on the IBIS specified range of Vcc to +2Vcc and -Vcc to Vcc respectively.

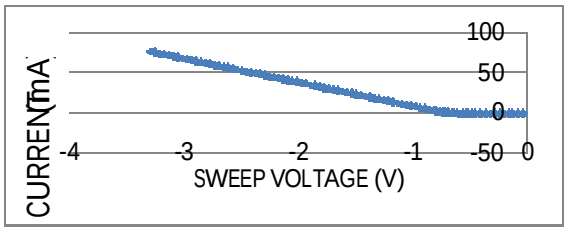

FIG. 3. Power clamp I/V curve referenced to V_{CC}.

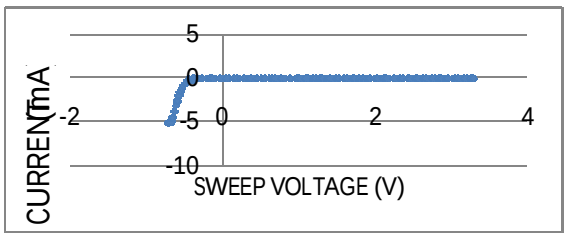

FIG. 4. Ground clamp I/V curve.

IIIb. The Pull-up and Pull-down I/V Curves

The Pull-up and Pull-down datas are only required to describe the characteristics of the output buffers, not for the input buffers. Some setting is first required before obtaining these curves, the output should be set to logic high state for pull-up curve and set to logic low state for the pull-down curve measurement. This setting is not required in the case of power and ground clamps because all the tri-state and the I/O buffers of the DUT are set in high impedance state to eliminate the effect of both the pull-up and pull-down transistors on the power and ground clamp data. A digital multi-meter was used to assure that the output voltage at the modeled pin had been set to the desired state. The output voltage of the buffer should indicate logic high for the pull-up and logic low for the pull-down.

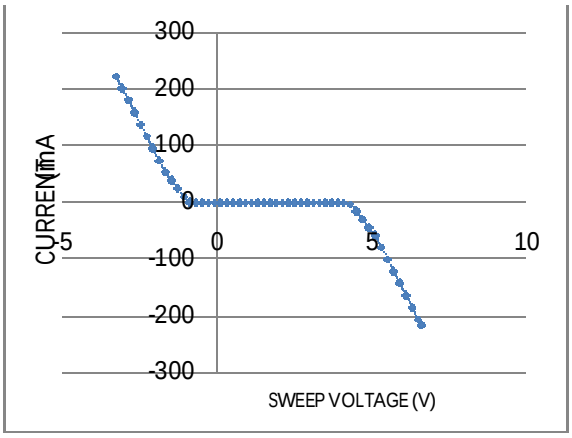

FIG. 5. Pull-up I/V curve.

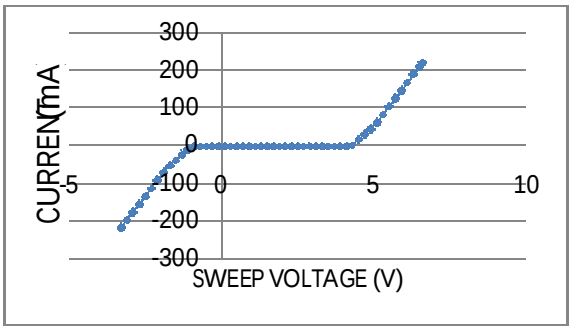

FIG. 6. Pull-down I/V curve.

```
|*************************************
|  Model io_pa
|*************************************
[Model] io_pa
Model_type I/O
Polarity Non-Inverting
Vinl= 0.8000v
Vinh= 2.000v
|
|variable typ min max
C_comp 5.00pF NA NA
|
|variable typ min max
[Voltage Range]3.3V NA NA
|
[Pulldown]
|voltage I(typ) I(min) I(max)
|
-3.30      -2.16E+02      NA      NA
-3.10      -1.95E+02      NA      NA
-2.90      -1.74E+02      NA      NA
-2.70      -1.53E+02      NA      NA
-2.50      -1.32E+02      NA      NA
-2.30      -1.11E+02      NA      NA
|
|
5.700      1.275E+02      NA      NA
5.900      1.488E+02      NA      NA
6.100      1.702E+02      NA      NA
6.300      1.915E+02      NA      NA
6.500      2.128E+02      NA      NA
6.600      2.234E+02      NA      NA
```

FIG. 7. An example of current-voltage result (pull-down clamp data).

IIIc. The Voltage-Time Data

V/T data describes the transient characteristics of the buffers. It is required only for the output and the I/O buffers, not for the input buffer, the I/O buffers should

be set to function as an output throughout the measurements. To toggle the output state from one to another, a trigger pin on the EVB was assigned to act as switch to drive the output pins into the desired logic state. If the trigger pin is tied to the Vcc, all the output pins will be automatically driven to logic high, when connected to Vss all output pins will be switched to logic low states. To capture the rising transient, the trigger pin was first connected to ground and then tied to Vcc; to capture the falling transient, the trigger pin was first tied to Vcc and then switch to Vss. The transient waveforms were displayed on the oscilloscope and the dV and dt values measured. Fig. 8 shows one example of the data obtained; it was seen that the ramp is 1.61/0.231 for the rising transient, and 1.63/0.327 for the falling transient.

```
-3.14    7.27E-02        NA      NA
-3.18    7.39E-02        NA      NA
-3.22    7.51E-02        NA      NA
-3.26    7.63E-02        NA      NA
-3.30    7.75E-02        NA      NA
                |
                |
             [Ramp]
|          typ            min     max
         |R_load = 50.00
                |
dV/dt_r  1.610/0.231    NA      NA
                |
dV/dt_f  1.630/0.327    NA      NA
                |
                |
|******End Model io_pa**********
```

FIG. 8. An example of RAMP result.

IIId. Putting Data into IBIS File

All the data obtained above must be put into the IBIS file, which is used in simulator. An IBIS file comprises three main components: (1) the Header information, (2) the device and pin information, and (3) I/V and V/T data for each model [4]. Fig. 9 shows the IBIS file for the DUT modeled.

For the device under test, it has three types of pins, viz. input pins, output pins, and the I/O pins. From the results of this work, it was found that the I/V characteristic curves for pull-up, pull-down, power clamp and ground clamp for the I/O pin and output pin are of the same values. Similarly the rising ramp for the I/O pin and output pin are of the same value; and so the falling ramp.

IV. CONCLUSIONS

In this paper, the step-by-step process to establish the IBIS model of the DUT was presented. Measurements of current-voltage and voltage-time relationship for the pull-up, pull down, power clamp and ground clamp of a 24 pin digital IC device was made and the results obtained successfully establishes the IBIS model of the device.

```
Header Information
  [IBIS Ver]  1.1
  [File Name] DUT.ibs
  [File Rev]  1.0
  [Date]  dd/mm/yy
  [Source]  obtained by physical measurement of the
device pins
  [Note]  this information is for sample file only

Device and Pin Information
  [Component] DUT
  [Manufacturer]  xxxxx
  [Package]  R_pin = 45m?
     L_pin = 2.5nH
     C_pin = 1.3pF
  [Pin]  refer to IBIS model

Modal data
  [Modal]  I, O, I/O
  [Vinl, Vinh]  0.8V, 2.0V
  [C_comp]  5.0pF
  [Ramp]  Variable  typ  min  max
   R_load = 50.00
   dV/dt_r 1.610/0.231 NA  NA
   dV/dt_f 1.630/0.327 NA  NA
 [End]
```

FIG. 9. The IBIS file for the DUT in this paper

REFERENCES

[1] IBIS Models: Background and Usage. Actel Corporation, http://www.actel.com/documents/Ibis_AN.pdf.

[2] Mark Chang, "Introduction to IBIS Modeling of Fiber Optic Transceivers", http://eesof.tm.agilent.com/pdf/ibis_background.pdf.

[3] IBIS (I/O Buffer Information Specification), http://www.eda.stds.org/pub/ibis.

[4] The IBIS Open Forum. IBIS Modeling Cookbook for IBIS Version 4.0, http://eda.org/pub/ibis/ver4.0/ver4_0.pdf.

[5] Company X. DUT User Manual and datasheet. Obtained From: Company X.