Transistor Characteristics of Semi Analytical 14 nm Gate Length Bi-GNMOS's

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Abstract. Bilayer graphene shows a remarkable physical property where its bandgap is tunable if an electric field is applied perpendicularly to the plane. This has overcome the problem of a single layer graphene in which the bandgap is difficult to be tuned. While researchers are showing interest in other transistor architecture such as FinFET and Trigate Field Effect Transistor, this paper has opted to explore on the enhancement of a conventional planar design by utilizing the graphene layers for which this is the first high performance planar transistor at 14-nm gate length. The development of a planar 14nm bilayer graphene top-gated n-type transistor was virtually fabricated and analyzed using SILVACO TCADS Tools. The model of bilayer grapheme transistor developed using SILVACO is a semi analytical model and it is suitable for exploring the process parameter in order to design a device structure with promising transistor performance. Our device, based on the effective mass calculation and ballistic transport assumption takes into account all relevant physical properties of bilayer graphene. The performance of the device was studied comprehensively and the performance was compared with that of the High-K/metal gate transistor. The device's simulation was carried out at fixed $V_{TH} = \pm 0.230$ V as guided by ITRS 2013. The results in the attainment of optimum V_{TH} show a better performance than High-K/metal gate transistor with $I_{ON} = 116.226$ μA/um, $I_{OFF} = 0.128636$ nA/um, DIBL=246.408 mV/V and SS = 134.652 mV/dec. Furthermore, this work highlighted the challenges of utilizing graphene-based devices for high performance digital applications and provided an optimized platform for future Graphene NMOS device enhancement.

Keywords: 14nm gate length; bilayer graphene; high-k dielectric; metal gate; SILVACO.

I. INTRODUCTION

The need to fabricate more transistors onto a single chip has resulted in the aggressive down scaling of transistors. In order to sustain Moore's Law while meeting the demand for high speed low power consumption, researches have been carried out for the implementation of new device geometries and new materials. This is in line with the International Technology Roadmap for

Semiconductors (ITRS) guidelines [1], which evaluates the technology essentials for the future generation of semiconductor devices including the processes for Metal Oxide Semiconductor Field Effect Transistor (MOSFET) technology.

However, the continuous down scaling of transistors for smaller devices is accompanied by several issues such as transport degradation in a transistor and parasitic effect. These issues have challenged the researchers and manufacturers to invent new solutions leading to the advancement of the technology from the conventional SiO_2/Poly-Si to the High-K/metal gate device and a planar device. Further work was carried out to explore on the finFET structure, which may not offer substantial performance below 22 nm node [2]. Subsequently, since its isolation in 2004, carbon allotropes, which are also known as graphene, have gained the attention of the researchers. Firstly, carbon nanotubes (CNT) has displayed a distinctive electronic and physical properties such as high mobility at room temperature and the potential for a wide range of applications [3]. However, CNT was banned for fabrication on the scale of integrated circuits (IC) due to the substantial gap in CNT for which it can only be obtained at a small width close to 1-2 nm [3].

Research was then extended to graphene layer and it quickly gained interest from the research community due to its low manufacturing costs and the ability to control the thickness of the channel at an atomic level. This can significantly improve the gate control over the channel barrier and hence reduce the Short Channel Effect (SCE) [4]. Graphene was extensively modelled theoretically and experimentally in [2-7] and was proven to be thermodynamically stable. The fact that graphene is a planar form draws a major advantage over CNT, because graphene permits for highly developed top-down CMOS-compatible process flows [8].

In this paper, we report the experimental results of a novel 14 nm bilayer graphene n-type planar transistors (Bi-GNMOS) with the utilization of High-K dielectric and metal gate as a top gate. This is the first work that reports on a set of new simulation results on 14-nm Bi-GNMOS that will serve as a useful simulation platform for future device enhancement. The device was virtually fabricated using ATHENA module and its performance characteristic was analyzed though ATLAS module where both modules are available in SILVACO TCADS Tools. The results were validated through the benchmarking with the High-K/metal gate transistor of the same gate length, displaying a better performance and can be enhanced for better Drain Induced Barrier Lowering (DIBL) and Subthreshold Swing (SS) through optimization process.

II. EXPERIMENT DESCRIPTIONS

A. Bi-GNMOS Virtual Fabrication

A planar 14-nm n-type MOSFET with a top-gated bilayer graphene transistor was simulated using the ATHENA module while its electrical characterization was studied via ATLAS module. The first step is to create a boron-doped Silicon substrate. Boron concentration was doped at $7x10^{14}$ cm^{-3} and thermally oxidized at 970 °C to a Silicon Dioxide (SiO_2) layer. The purpose was to suppress the short channel effect (SCE) caused by the expansion of the depletion layer within the substrate.

Next, a bilayer of doped-graphene was deposited on top of the SiO_2 by using a conformal method. It was assumed that the bilayer doped-graphene displays no defects and it possesses a ballistic transport property. Hence, the channel width was neglected in this research. The thickness of the bilayer graphene was decided based on [4, 9] and was presumed for these devices in the simulations. A thickness of 0.67 nm High-k materials, Hafnium Dioxide (HfO_2)

was then deposited on top of graphene layers followed by a 38 nm thickness of Tungsten Silicide (WSi_2) metal gate on the dielectric layer. Both were etched accurately to produce a gate length of 14 nm (±0.1 nm) transistor. To reduce the short channel effect (SCE), Halo implantation is doped with Indium at $1.159x10^{14}$ cm^{-3} dopant value.

Arsenic was then implanted at a high dopant concentration of $1.328x10^{14}$ cm^{-3} to accumulate the Schottky tunneling of the source-drain (S/D) regions. This created a low resistive track for only electrons or holes to be injected into the graphene channel to achieve a unipolar conduction. The final process took place after the growth of 0.015 um Borophosphosilicate Glass (BPSG) and Phosphor doped at $0.65x10^{14}$ cm^{-3} for Compensation implantation where the metal contact was formed and etched accordingly using Aluminum layer. The device was finally ready for its electrical characterization and performance analysis using ATLAS module. Figure 1 shows the doping profile of the 14 nm bilayer graphene n-type transistors where graphene layer is characterized in yellow color, HfO_2 in purple and it is sandwiched between the graphene and WSi_2 layers. Although the design edges are slightly vacillated, the separation between source and drain can be clearly seen.

B. Semi Analytical Design for Bilayer Graphene

To study and evaluate the electrical characteristics of the transistor, simulations were carried out using ATLAS module, in which all the physical properties of the graphene layers were considered. The operation was presumed at room temperature (T = 300 K). In the analysis, the graphene layers were modeled as a semi-metal with a bandgap of around 0.55 eV [5], a dielectric constant of 2.4 [8], a carrier mobility of top-gated measured at a room temperature and effective field of E_{eff} = 0.4 MV/cm [8]. The radiative recombination rate of electrons and holes in graphene layer were set at a relatively large value of 100 ns [9]. The graphene's 2-Dimensional (2D) electrons and holes densities of states were measured at room temperature and obtained from [9]:

$$Nc = \frac{8\pi m_e kT}{h^2} \ln\left(1 + e^{-(Ec-Ef)/kT}\right)$$
$$Nv = \frac{8\pi m_e kT}{h^2} \ln\left(1 + e^{-(Ec-Ev)/kT}\right) \quad (1)$$

where the effective masses of electrons and holes in graphene, were set at $m_e \approx 0.06\ m_o$ and $m_h \approx 0.03 m_o$ while m_o is the free electron mass. The values of these parameters followed those used in [4]. The number of electrons and holes per unit area was experimentally measured to be around 10^{12} cm^{-2} at room temperature which also satisfies (1) [9].

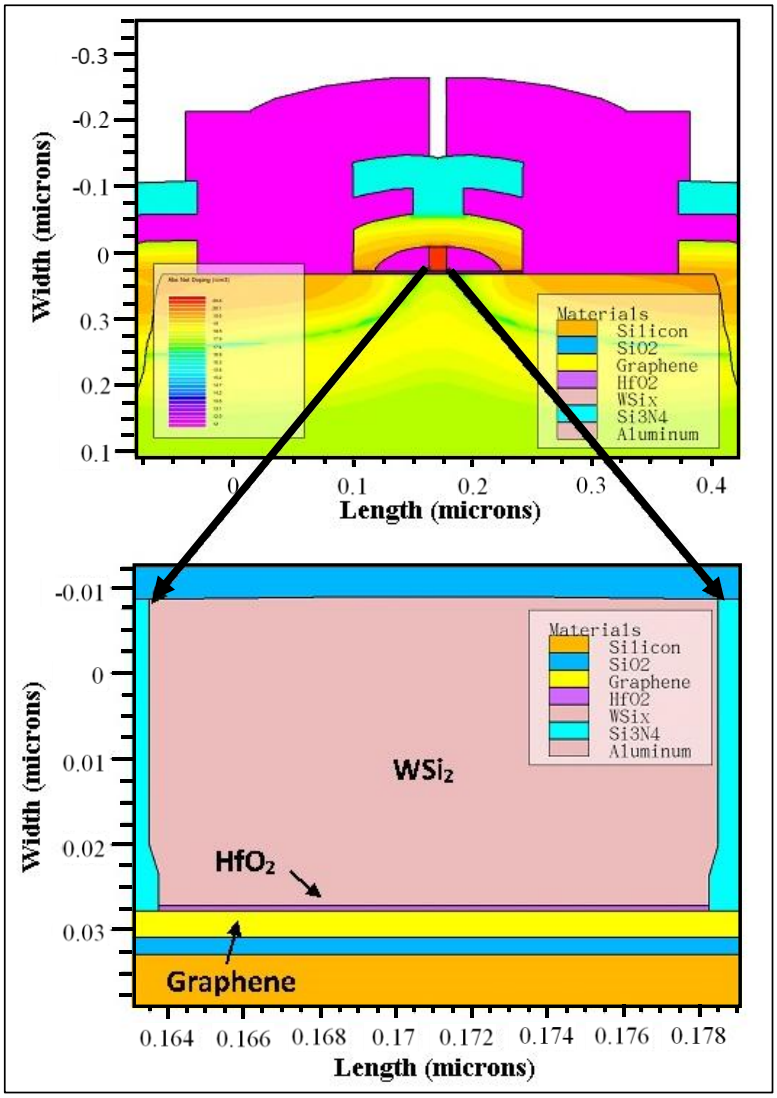

FIGURE 1. Doping Profile of 14 nm Bi-GNMOS

C. Results and Discussion

The electrical characteristics of a planar 14 nm bilayer doped-graphene n-type transistor with High-K dielectric and metal gate as a top gate were simulated through ATLAS module. In achieving the target of designing a high-performance device with low power consumption, the performance measurement focused on the on-state current (I_{ON}), leakage current (I_{OFF}), the switching capability of the device through the I_{ON}/I_{OFF} ratio, subthreshold swing (SS) and Drain Induced Barrier Lowering (DIBL). To strengthen the findings, threshold voltage (V_{TH}) was set at 0.230 V according to the ITRS 2013 for 14 nm gate length [1]. To achieve the target of V_{TH}=0.230 V, several control factors were varied in these simulations which included the doping concentration of Halo Implant, S/D Implant, Compensation Implant and annealing temperature [10, 11]. Figure 2 shows the drain current I_D versus the drain voltage V_D characteristic at various gate voltage VG of 0.1 V, 1.0 V, 2.0 V and 3.0 V. Figure 3 shows the sub drain current I_D versus the gate voltage V_G characteristic and Figure 4 shows the drain current I_D versus the gate voltage

V_G characteristic at drain voltage V_D of 0.5 V and 1.0 V with the inset showing the determination of V_{TH}. V_{TH} value is measured from these characteristic curves.

From the simulated results in Figure 3, I_{OFF} is 0.128636 nA/um at V_D=0.5 V and I_{ON} is 116.226 uA/um at V_G=1.0 V. Furthermore, the 14 nm n-type bilayer graphene transistor exhibits almost 99.8% lower leakage current than that of the High-K/metal gate transistor [12] with the same gate length. One of the properties of graphene, which is the high electrons and holes mobilities, enables the transistor to go into saturation regions very quickly, despite the large electron saturation velocities [2]. As can be seen in Figure 2, I_D increases as V_G increases and reaches saturation at V_D greater than 0.12 V. The metric performances of 14 nm bilayer doped-graphene n-type transistors are summarized in Table 1 and they are compared against the 14 nm High-K/metal gate NMOS [12]. In comparison with a modern MOSFET which has a SS of about 90 mV/dec and the theoretical limit of 60 mV/dec [13], this structure has a higher SS of about 134.652 mV/dec. The result also shows a very high DIBL. The reason of the high SS and DIBL is due to the high holes concentrations of graphene in the subthreshold region. The depletion layer is increased due to high substrate doping concentration which also leads to the additional loss and the bigger tunneling area contributed by the junction depth. High value in junction depth allows high amount of current to be tunneled from this area of the junction [14].

The advantage of bilayer graphene, which has high electron mobility and conductivity, causes the device hard to be switched off [2-5]. However, it allows the device structure to be scaled down on top of Moore's Law and having better control of the gate voltage on the channel region by tuning the bandgap [3]. The employment of high number of dopants in the S/D regions which forms a Schottky tunneling junctions also resulted in high on-state current (I_{ON}) [15]. This is proven when Bi-GNMOS shows an on-state current (I_{ON}) of 116.226 μA/μm. Although the I_{ON} is still below of that predicted by ITRS 2013, it is higher than that of benchmarked High-K/metal gate Silicon transistor. Nevertheless, a more crucial performance parameter is the I_{ON}/I_{OFF} ratio because it determines the switching capability of the transistor. In this context, the Bi-GNMOS demonstrated an I_{ON}/I_{OFF} ratio that is higher than those predicted by ITRS 2013 and the benchmarked devices. This is mainly due to the very low leakage current (I_{OFF}) of Bi-GNMOS at 0.128636 nA/μm, which is significantly lower than 77.11 nA/μm of the High-K/metal gate transistor.

The I_{OFF} of Bi-GNMOS is limited by constraining the graphene by the utilization of Hafnium Dioxide (HfO_2) dielectric (k~22). The I_{ON} to I_{OFF} ratio of the Bi-GNMOS, which is two times higher than that of the High-K/metal gate device, also demonstrated that Bi-GNMOS is more superior. This is due to the bandgap opening of boron-doped bilayer graphene replacing the carbon (C) atoms. The result of I_{ON}/I_{OFF} indicates that Bi-GNMOS has a better switching capability and it is extremely desirable for high performance logic circuits as Bi-GNMOS possesses I_{ON}/I_{OFF} that is higher than that of the ITRS requirements at 10^4.

TABLE (1). Performance Analysis of 14 nm Bi-GNMOS.

Performance Parameter	ITRS 2013 Prediction	High-K/metal gate NMOS [12]	Bi-GNMOS
V_{TH} (V)	0.230	0.232291	0.23011
I_{ON} (μA/μm)	> 1267	78.922	116.226
I_{OFF} (nA/μm)	< 100	77.11	0.128636
I_{ON}/I_{OFF} Ratio	> 1.27×10^4	1.023×10^3	9.03×10^5

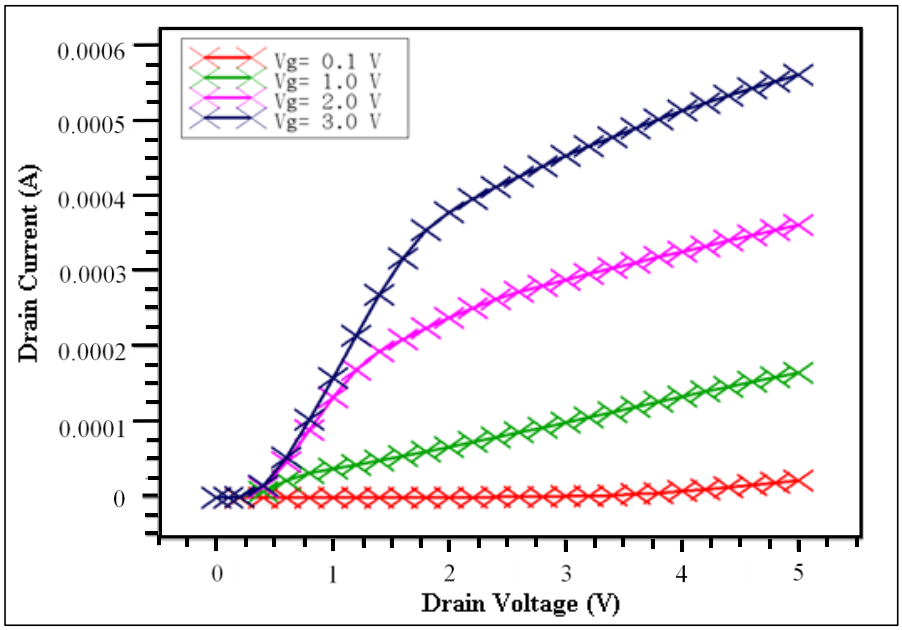

FIGURE 2. Graph of I_D-V_D for 14 nm Bi-GNMOS.

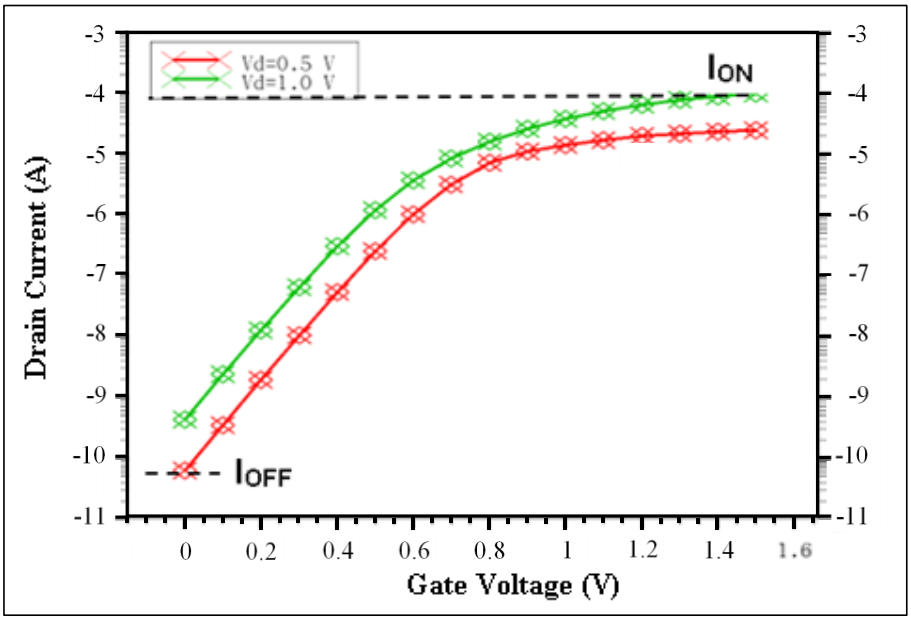

FIGURE 3. Graph of Sub I_D-V_G for 14nm Bi-GNMOS

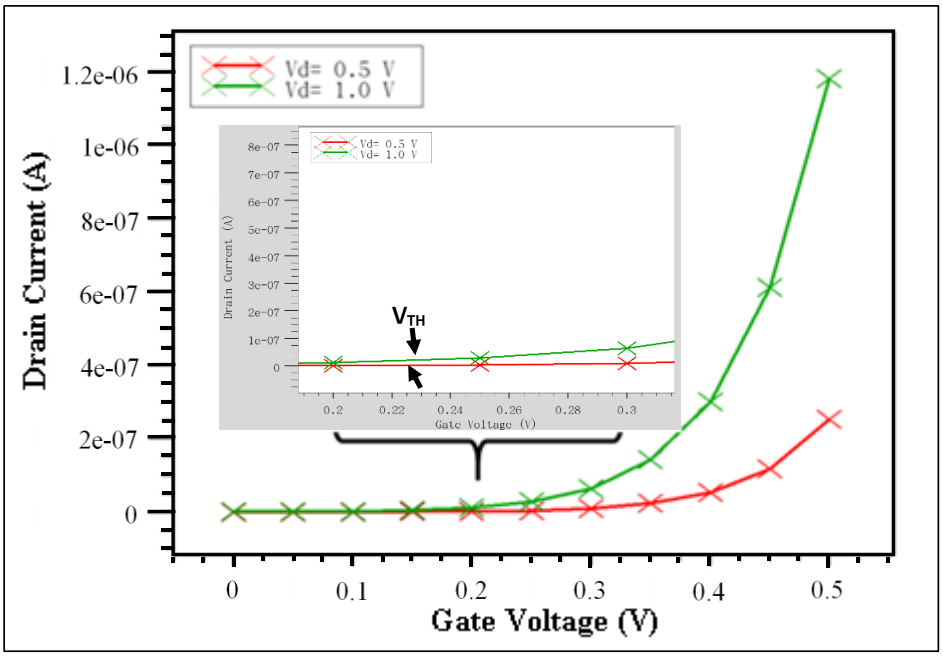

FIGURE 4. Graph of I_D-V_G for 14nm Bi-GNMOS with The Inset Showing the Determination of V_{TH}

D. Conclusion

A virtual model of 14 nm Bi-GNMOS n-type transistor was successfully fabricated in this research and the significant features of Bi-GNMOS performance were confirmed through benchmarking and comparison with High-K/metal gate transistor of the same gate length which is suitable for the exploration of the design parameters. The device was also designed based on the assumption of an ideal bilayer graphene that possesses ballistic transport property. Despite a very small gate length, Bi-GNMOS also displayed a transistor operation at room temperature. The device was also shown to be well-matched with the High-K dielectric which indicated that the gate dielectric scaling beyond the limits of SiO_2 is possible to be implemented. Due to the high DIBL and SS as compared to the theoretical limit, further numerical work is necessary to enhance the transistor performance with optimum value of doping concentrations.

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1. ITRS 2013 Report; http://www.itrs.net.
2. G. Fiori, F. Bonaccorse, G. Iannaccone et al., *Rev. Article Nature Nanotechnology* **9** (2014).
3. M. Cheli, G. Fiori and G. Iannaccone, *IEEE Transactions on Electron Devices* **56**, 2979-2986 (2009).

4. A.C. Ferrari, J.C. Meyer, V. Scardaci, C. Casiraghi et. al., *Phys. Rev. Lett.* **97**, 187401-1-187401-4 (2006).
5. P. Nemes-Incze, Z. Osva´ th, K. Kamara´ s, L.P. Biro´, *Carbon* **46**, 435-1442 (2008).
6. A. Hamzah, A.S. Azman, R. Ismail et al., *Proceedings of the IEEE Regional Symposium on Micro and Nanoelectronics*, 1-4 (2015).
7. K. Tamersit, F. Djeffal, D. Arar and M. Meguellati, *Proc. of the WCE* **II** (2013).
8. B. Guo, L. Fang et al., *Insciences J.* (2011).
9. K.S. Novoselov, A.K. Geim, S.V. Morozov, D. Jiang, et. al., *Science* **306**, 666-669 (2004).
10. H.A. Elgomati, B.Y. Majlis, A.M.A. Hamid, P.S. Menon, and I. Ahmad, *Proceedings of the Sixth International Conference on Mathematical Modelling and Simulation* 40–45 (2012).
11. A.M.A. Hamid, P. S. Menon, I. Ahmad, S. Shaari, H.A. Elgomati, B.Y. Majlis, F. Salehuddin, *Australian Journal of Basic and Applied Sciences* **6**, 1-8 (2012).
12. Z.A.N. Faizah, I. Ahmad, P.J. Ker et. al., *Proceedings of the IEEE Regional Symposium on Micro and Nanoelectronics* (2015).
13. N. Ghobadi and M. Pourfath, *IEEE Transactions on Electron Devices* **61**,186-192 (2014).
14. M. F. Al-Mistarihi, A. Rjoub, and N. R. Al Taradeh, *IEEE Transactions on Electron Devices* (2013).
15. J. Zhu, J.C.S. Woo, *IEEE Transactions on Electron Devices*, 243-246 (2007).